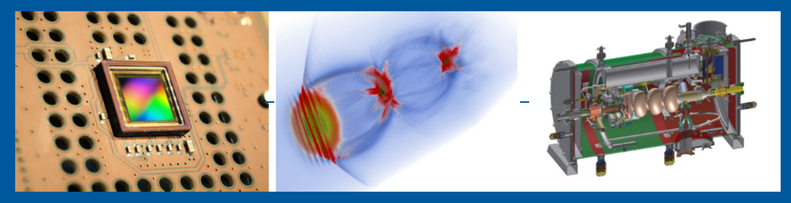
Programme Matter and Technologies

CMS L1 Track Trigger Hardware Demonstrators



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Motivation: High Luminosity LHC

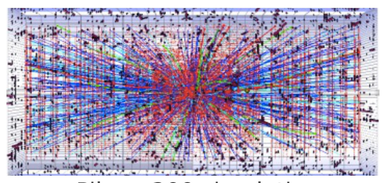
▸ By 2026 - **LHC** will be **upgraded** in **luminosity** -> 2-3x improved statistics by 2035 vs no upgrade

▸ **Tracker will be replaced** (radiation damage) - Phase II CMS

▸ Challenging high occupancy conditions, **~15,000 tracks per bx**, must perform ≥ at present

▸ **New design** will allow tracker to **read out a sub-set of data at 40 MHz**

▸ Completely **new handle** at L1 trigger, to keep rate < 750 kHz, while maintaining sensitivity to interesting physics



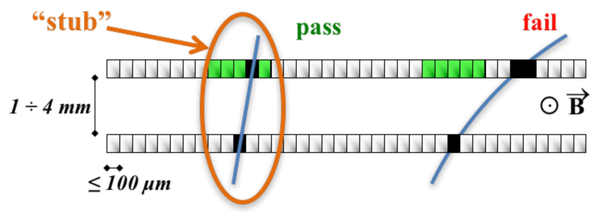
Pileup 200 simulation

CMS Tracker Upgrade

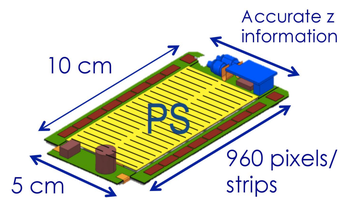
▸ High p_T tracks signs of interesting physics (decays of high mass particles)

▸ **Novel tracking modules** utilise two **1.6-4.0 mm spaced silicon sensors**, to **discriminate p T > 2-3 GeV**

▸ Forward these **stubs** to **off-detector trigger electronics** - rate reduction O(100)



"PS" Pixel + Strip Modules 20 < r < 60 cm



Strip Sensor × 2: 2. 5 cm × 100 μm

+

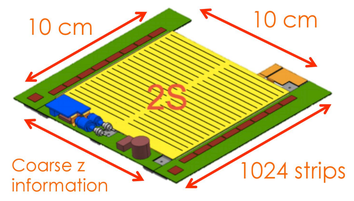
Pixel Sensor × 32: 1.5 mm × 100 μm

"2S" 2 Strip Modules r > 60 cm

Strip Sensor × 2: 5 cm × 90 μm

+

Strip Sensor × 2: 5 cm × 90 μm



The Track Finding Processor (TFP)

▸ Total available L1 time will be 12.5 µs, but **only ~4 µs is available for track finding**

▸ Must construct a track finder that is capable of processing **very high data rates (~20,000 stubs per event)** down to the O(10) genuine/ interesting tracks expected on average, within this latency target

▸ **Proposal: Track Finding Processor (TFP)** receive data links from adjacent detector octants in φ

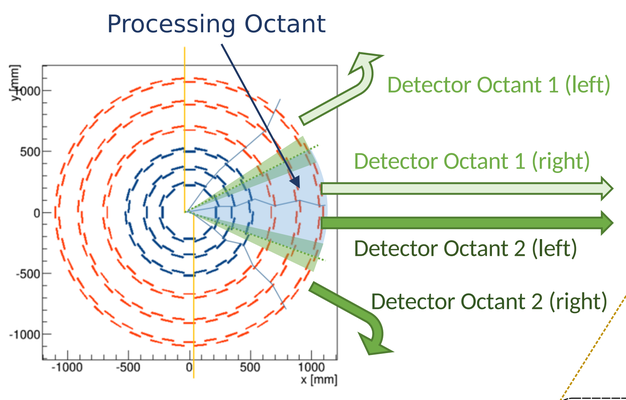
▸ Fully **time-multiplexed system**: Processing of subsequent events done on parallel independent nodes

▸ **Highly scalable system**

▸ Each TFP processes **1/8 in φ and 1/tmp** (time multiplex period) in time

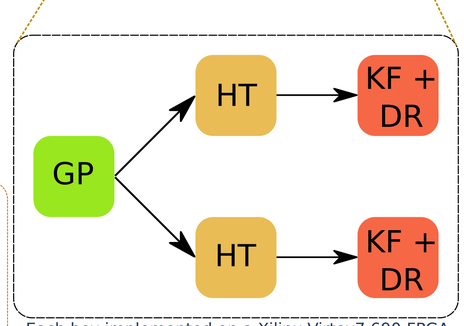
▸ One TFP become the **demonstrator slice unit**

FPGA based Hardware Demonstrator



Geometric Processor (GP) - processes stub data, and sub-divides the octant into 36 finer sub-sectors

Hough Transform (HT) - A highly parallelized first stage track-finder that identifies groups of stubs consistent with a track in the r-φ plane

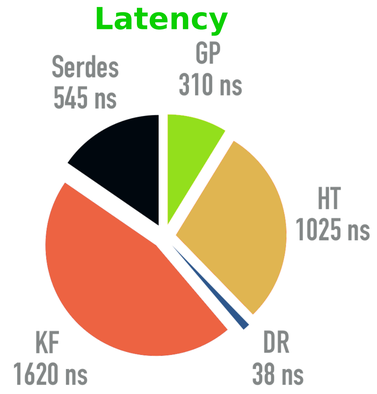


Each box implemented on a Xilinx Virtex7 690 FPGA

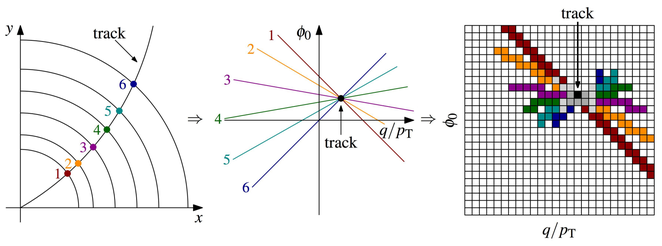
Kalman Filter (KF) - A candidate cleaning and precision fitting algorithm

Duplicate Removal (DR) - Uses precise fit information to remove duplicate tracks generated by the HT

Latency



The r-φ Hough Transform (HT)



▸ Search for **primary tracks in the r-φ plane**, using the **parameterisation (q/ p_T , $φ_0$)**

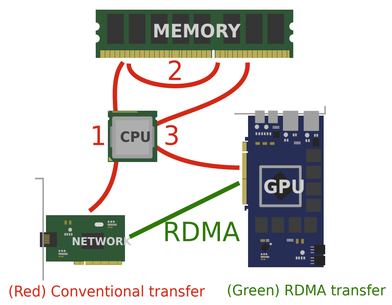
▸ **Stub positions correspond to straight lines in Hough Space**

▸ **Where 4 or more lines intersect -> track candidate**

Heterogeneous Hardware Demonstrator

▸ Remote Direct Memory Access (RDMA) can be used to **directly connect GPUs with FPGAs**

▸ This allows for **highly flexible FPGA-based DAQ** hardware combined with the high performance computing **GPUs**



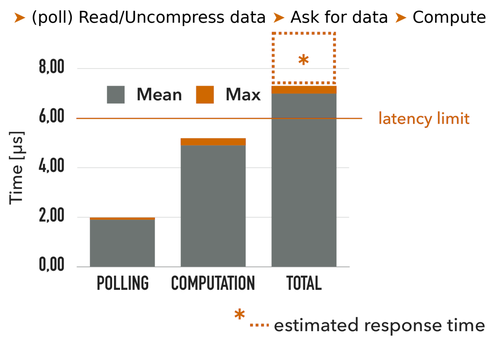
r-φ Floating Point Hexagonal HT

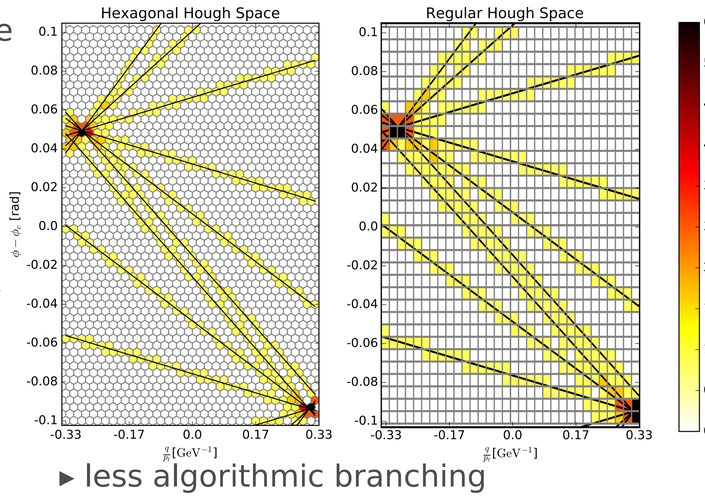
▸ Hexagonal bins in hough space

▸ **Suppresses fake** candidates in **80%**

▸ Runtime comparable

▸ **only 1 possible bin per row**





▸ less algorithmic branching

▸ Computational time of around **4 µs**

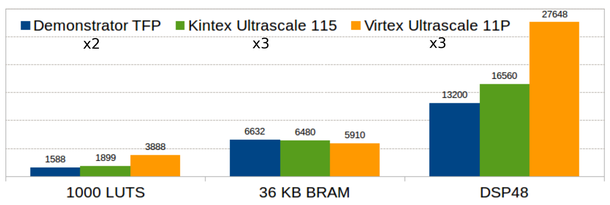
▸ More **complex algorithms** are possible: hexagonal approach

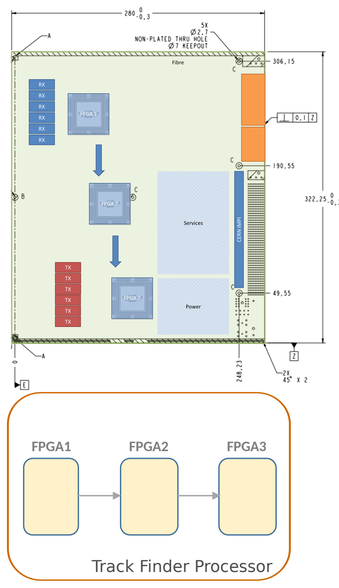
Future FPGA Demonstrator Development

▸ Future work will be to build a system using the **KU115 FPGA** and **16.3 Gbps optical links** with a target latency of 2 µs using the **ATCA** form factor

▸ Targeting **18BX** would have the same volume of data at twice the rate => **needs 2x processing capacity**

▸ Total sum of logic needed would be **O(3) KU115 FPGAs**





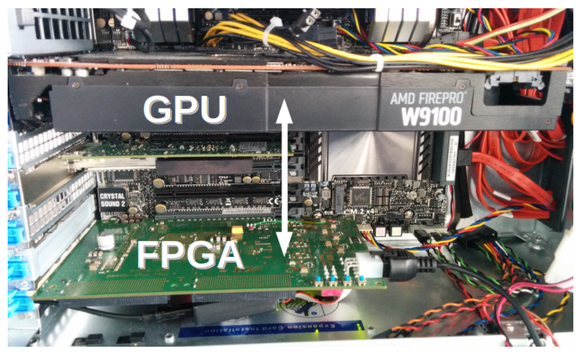
Outlook of Heterogeneous Demonstrator: fast feedback loops

▸ RDMA enables **low-latency** data-transfers

▸ Paired with efficient algorithms, GPUs can be used to realize **tight feedback loops** with less than **10µs latency!**

▸ We ilustrate the performance of such systems by a **prototype implementation** of the L1 CMS Track Trigger HT

▸ Look at performance of newer GPUs
- High Bandwidth Memory **(HBM) 2-4x** better throughput



▸ Investigate new transfer technologies
- PCIe 4.0 (**2x** faster)
- NV-Link (**5-10x** faster)